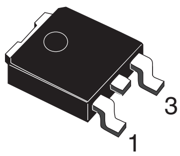
STD25NF10L

N-channel 100V - 0.030Ω - 25A - DPAK
Low gate charge STripFET™ II Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STD25NF10L	100V	< 0.035Ω	25A

- Exceptional dv/dt capability
- 100% avalanche tested
- Low threshold device
- Logic level device

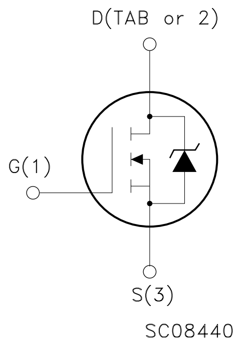


DPAK

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STD25NF10LT4	D25NF10L	DPAK	Tape & reel

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	100	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	100	V
V_{GS}	Gate- source voltage	± 16	V
I_D(1)	Drain current (continuous) at T_C = 25°C	25	A
I_D	Drain current (continuous) at T_C = 100°C	21	A
I_{DM}(2)	Drain current (pulsed)	100	A
P_{tot}	Total dissipation at T_C = 25°C	100	W
	Derating Factor	0.67	W/°C
dv/dt(3)	Peak diode recovery avalanche energy	20	V/ns
E_{AS} (4)	Single pulse avalanche energy	450	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature		

1. Current limited by package
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 25A$, di/dt ≤300A/µs, $V_{DD} = V_{(BR)DSS}$, $T_j \leq T_{JMAX}$
4. Starting T_j = 25 °C, I_D = 12.5A V_{DD} = 50V

Table 2. Thermal data

Rthj-case	Thermal resistance junction-case max	1.5	°C/W
Rthj-pcb	Thermal resistance junction-pcb max (1)	100	°C/W
T_J	Maximum lead temperature for soldering purpose	275	°C

1. When Mounted on 1 inch2 FR-4 board, 2 oz of Cu.

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS} =0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 16V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 12.5A V_{GS} = 4.5V, I_D = 12.5A		0.030 0.035	0.035 0.040	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15V, I_D = 12.5A		24		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1MHz, V_{GS} = 0		1710 250 110		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 50V, I_D = 12.5A R_G = 4.7Ω V_{GS} = 5V (see *Figure 13*)		20 40 58 20		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 80V, I_D = 25A, V_{GS} = 5V, R_G = 4.7Ω (see *Figure 14*)		38 8.5 21	52	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				25 100	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 25A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 25A, di/dt = 100A/µs, V_{DD} = 50V, T_j = 150°C (see *Figure 15*)		88 317 7.2		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

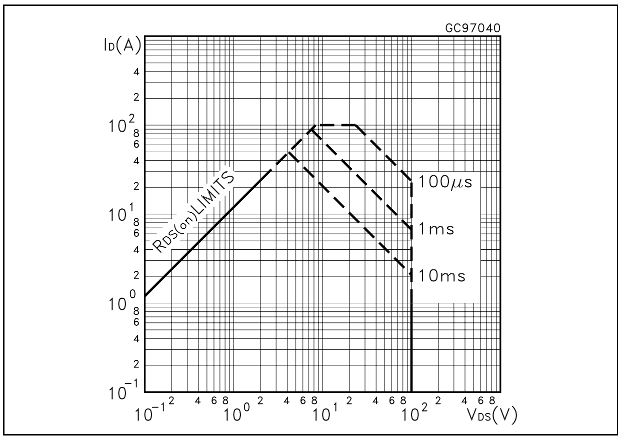


Figure 2. Thermal impedance

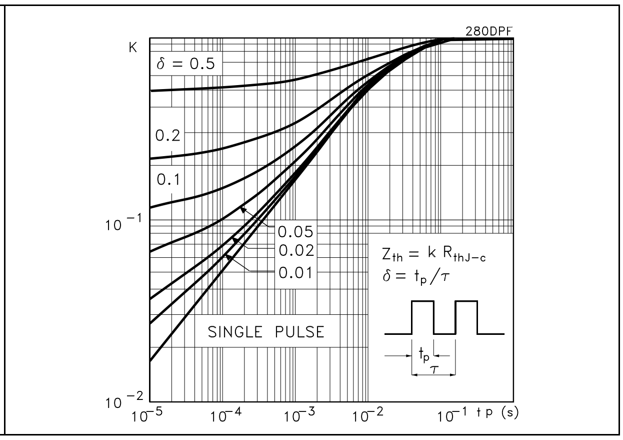


Figure 3. Output characterisics

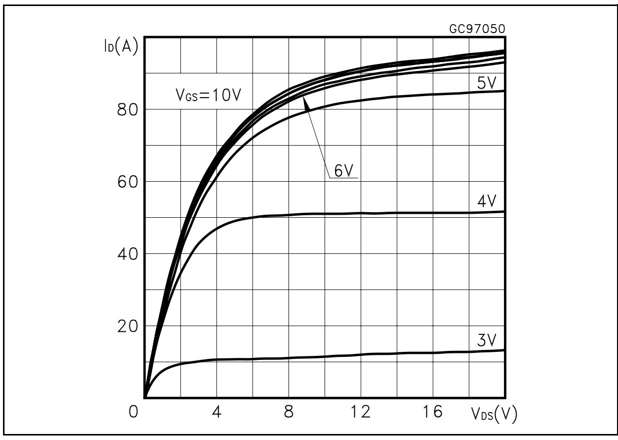


Figure 4. Transfer characteristics

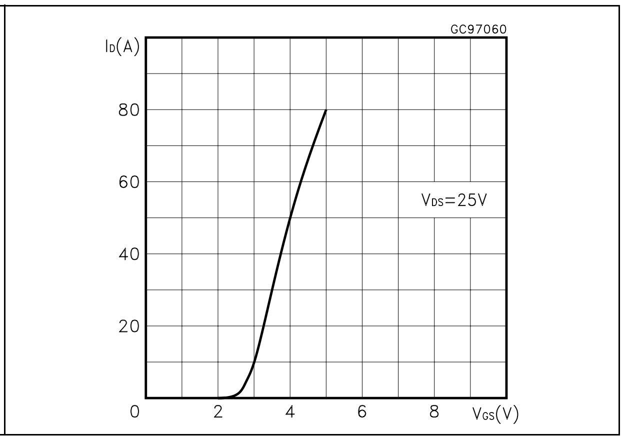


Figure 5. Transconductance

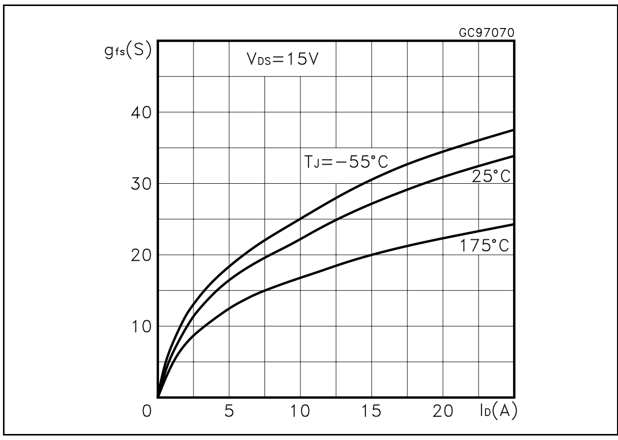


Figure 6. Static drain-source on resistance

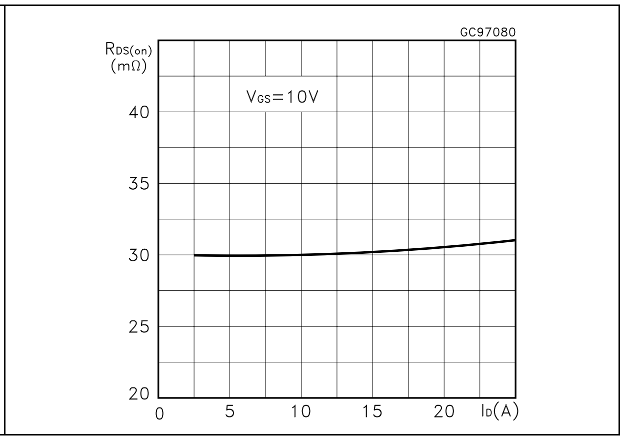


Figure 7. Gate charge vs gate-source voltage

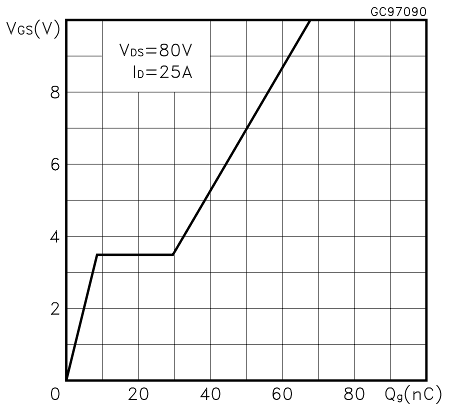


Figure 8. Capacitance variations

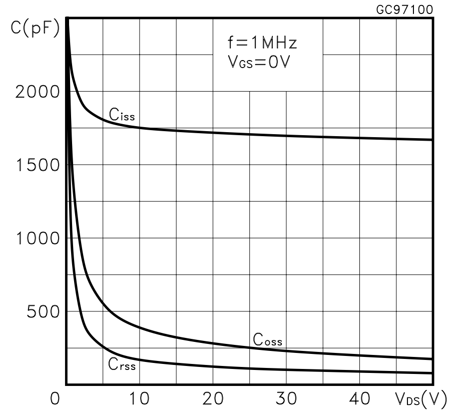


Figure 9. Normalized gate threshold voltage vs temperature

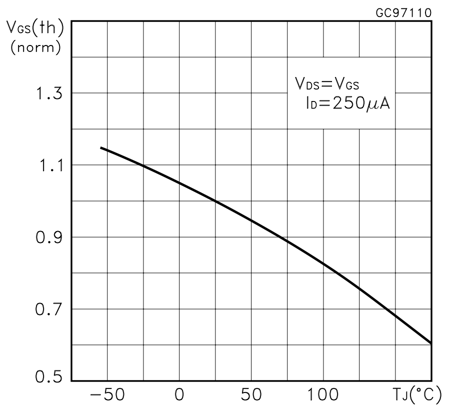


Figure 10. Normalized on resistance vs temperature

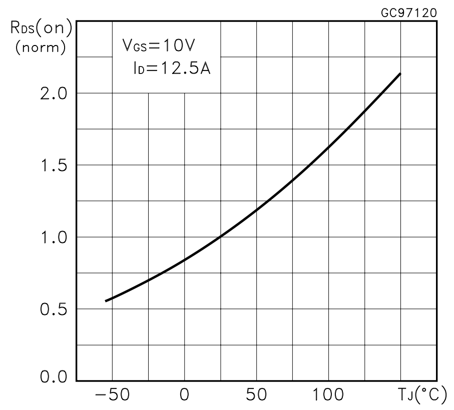


Figure 11. Source-drain diode forward characteristics

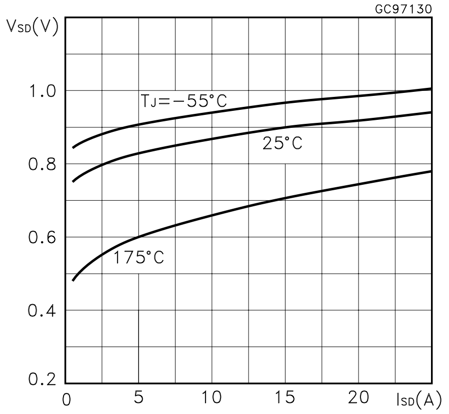
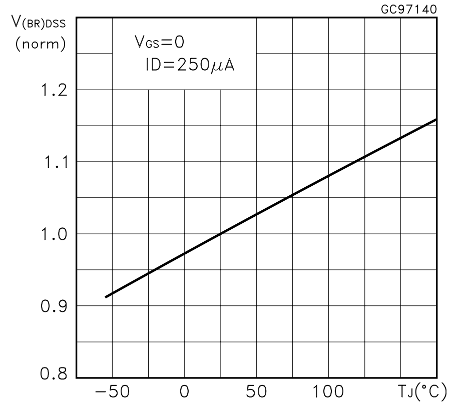


Figure 12. Normalized breakdown voltage vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

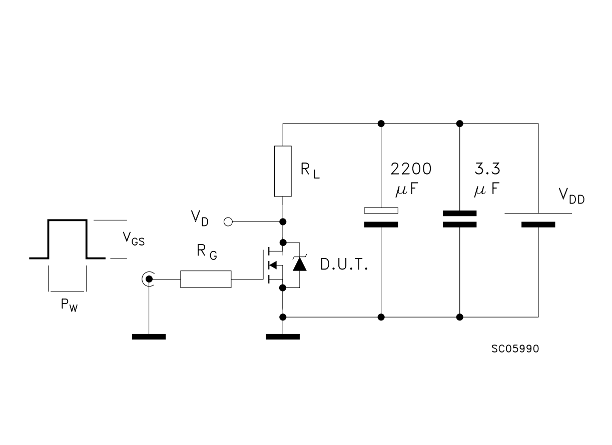


Figure 14. Gate charge test circuit

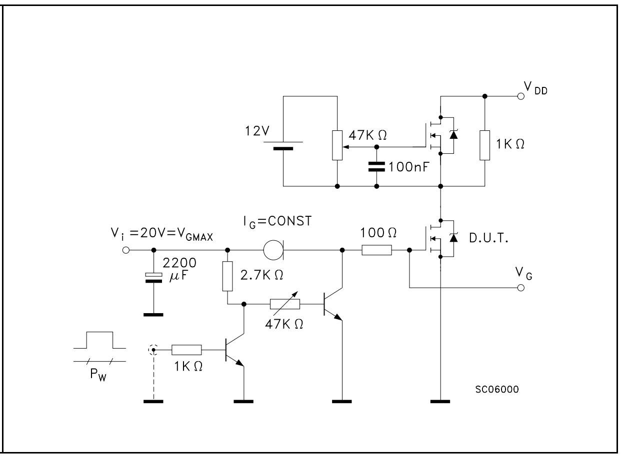


Figure 15. Test circuit for inductive load switching and diode recovery times

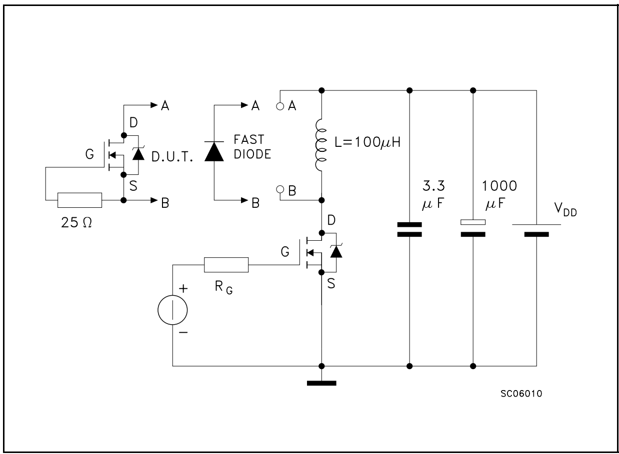


Figure 16. Unclamped Inductive load test circuit

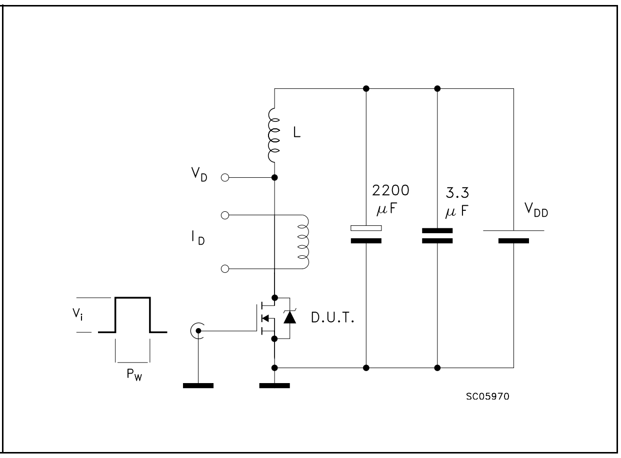


Figure 17. Unclamped inductive waveform

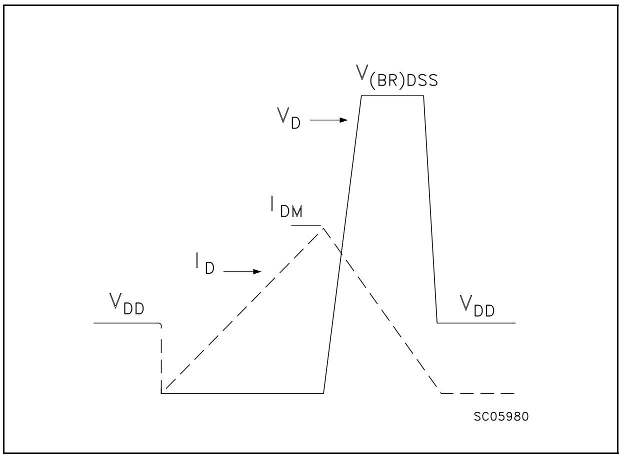
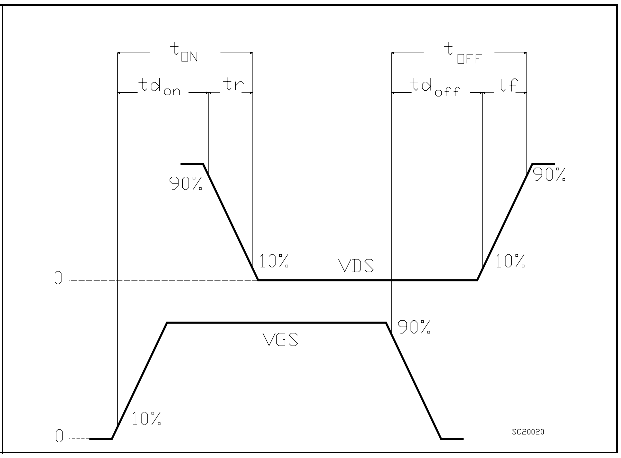


Figure 18. Switching time waveform

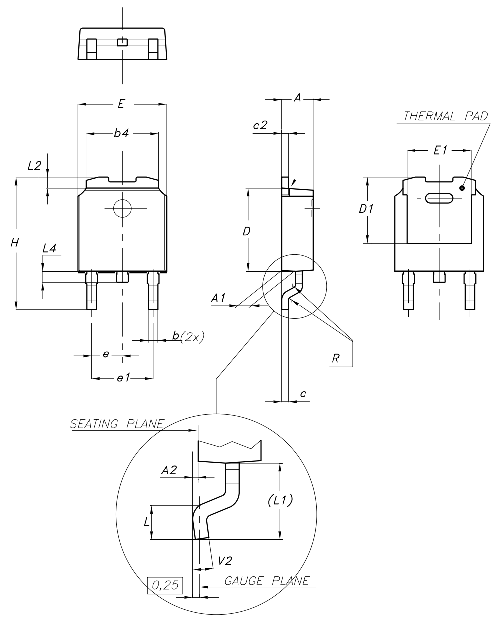


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

DPAK MECHANICAL DATA

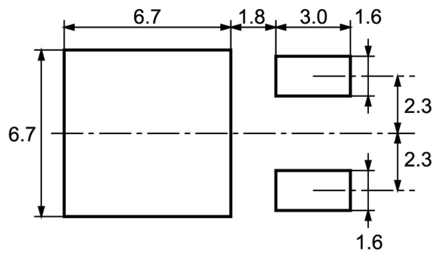
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



0068772-F

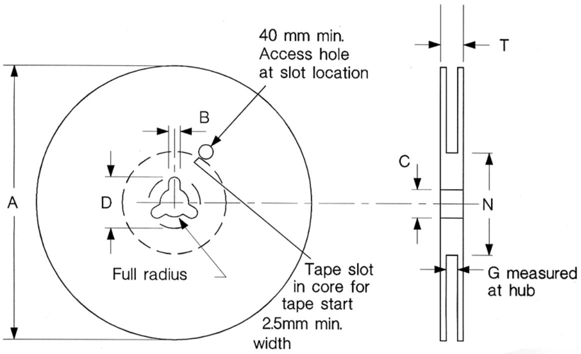
5 Packing mechanical data

DPAK FOOTPRINT



All dimensions are in millimeters

TAPE AND REEL SHIPMENT



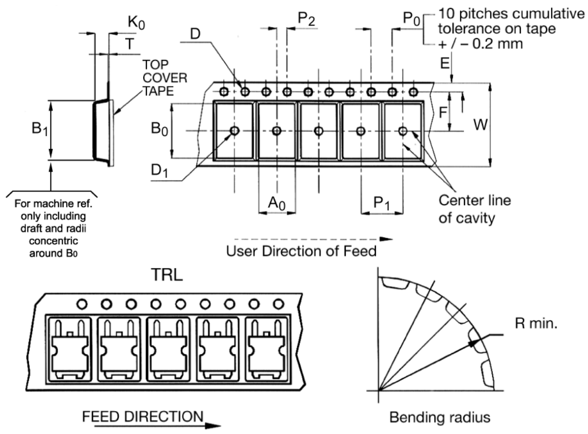
REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641



6 Revision history

Table 6. Revision history

Date	Revision	Changes
21-Jun-2004	1	Preliminary version
03-Jun-2006	2	New template, no content change